SEMESTER S7

POWER-EFFICIENT VLSI ENGINEERING

Course Code	**PEEVT 745**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	5/3	**Exam Hours**	2 Hrs.30 Min.
Prerequisites (if any)	PCECT302 Solid State Devices	**Course Type**	5 Credit Elective

Course Objectives:

1. To equip students with a comprehensive understanding of power dissipation mechanisms in MOSFET devices, the necessity for low-power circuit design, the challenges associated with deep submicron transistor design, and the exploration of emerging low-power technologies
2. To enable students to analyse the various sources of power dissipation in digital ICs, including dynamic, short circuit, switching, glitching, and static power, and to understand the impact of design parameters on power efficiency.
3. To provide students with an in-depth understanding of low-power design approaches, including supply voltage scaling, architectural techniques, and advanced methods for reducing leakage power and improving clock distribution efficiency.
4. To equip students with the knowledge of various low-power circuit design styles, including non-clocked and clocked approaches, adiabatic switching, and energy recovery techniques, to minimize power consumption in VLSI circuits.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Physics of Power dissipation in MOSFET devices** Need for low power circuit design, MIS Structure **Deep submicron transistor design issues: Short channel effects** Channel Length Modulation , Surface scattering, Punch through, Velocity	9

	saturation, Impact ionization, Hot electron effects, Body Effect, Narrow width effect, V_{th} roll-off, Drain Induced Barrier Lowering, Gate Induced drain leakage, Tunneling Through Gate Oxide, Subthreshold Leakage Current, **Emerging Technologies for Low Power:** Hi-K Gate Dielectric, Lightly Doped Drain–Source, Silicon on Insulator	
2	**Sources of power dissipation in digital ICs** – **Dynamic Power Dissipation:** Short Circuit Power: Short Circuit Current of Inverter , Short circuit current dependency on input rise and fall time, Variation of shortcircuit current with load capacitance. Switching power dissipation: Switching Power of CMOS Inverter, Switching activity and its effects. Glitching Power: Glitches and its effect on power dissipation **Static Power Dissipation:** Sources of Leakage Power, Effects of V_{dd} and V_t on speed, Constraints on V_t Reduction.	9
3	**Low-Power Design Approaches-** **Supply Voltage Scaling for Low Power:** Effect of Supply voltage on Delay and Power Effect of Supply voltage on Static and Dynamic Power Multi VDD ,Dynamic VDD, Dynamic Voltage and Frequency Scaling (DVFS) Approaches. Architectural Level Approaches: Pipelining and Parallel Processing **Leakage power reduction Techniques:** Effect of threshold voltage on Leakage Power Transistor stacking, MTCMOS, VTCMOS Power gating& Clock gating Techniques. Power-Efficient Clock Distribution	9

4	**Circuit Design Styles for Low Power-** **Non clocked circuit design style:** Fully Complementary logic. NMOS and Pseudo –NMOS logic, Differential Cascode Voltage Switch logic(DCVS) **Clocked design style:** Basic concept, Dynamic Logic, Domino logic, Differential Current Switch Logic. **Adiabatic switching** – Adiabatic charging, Adiabatic amplification, Adiabatic logic gates, Pulsed power supplies. Energy Recovery Circuit Techniques	9

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Internal Ex	Evaluate	Analyse	Total
5	**15**	**10**	**10**	**40**

Criteria for Evaluation (Evaluate and Analyse): 20 marks

1. Literature Review and Report (10 Marks)

Assessment Method:

- Students select recent publications on a specific topic related to the course (eg. Hi-K Gate Dielectrics).
- Preparation of a report summarizing the findings, discussing the significance, and proposing future research directions.

Criteria:

- Relevance of Chosen Publications (2 Marks): Selection of up-to-date and significant research papers.
- Depth of Analysis (4 Marks): Thorough understanding and critical analysis of the literature.
- Clarity and Organization (2 Marks): Well-structured report with clear arguments.
- Originality (2 Marks): Innovative insights or perspectives.

2. Design Exercise (5 Marks)

Assessment Method:

- Design a basic adiabatic logic gate (e.g., AND, OR, XOR) using a simulation tool such as Cadence or HSPICE, simulate the circuit, analyze the power consumption, and compare it with a conventional CMOS logic gate.
- Preparation of a detailed report.

Criteria for Assessment (Total: 5 Marks):

- **Correctness of the Design (2 Marks)**:
  - The logic gate must function correctly, with accurate simulation results that match the expected logical behavior.
- **Power Consumption Analysis (2 Marks)**:
  - Students should provide a comparative analysis showing how the adiabatic logic gate consumes less power compared to a traditional CMOS gate. This should include quantitative data from the simulation.
- **Clarity and Completeness of the Report (1 Mark)**:
  - A concise report detailing the design process, simulation setup, results, and conclusions. The report should be well-organized and clear, making it easy to follow the student's work.

4. Case Study Analysis (5 Marks)

Assessment Method:

Task: Students will be given a case study that involves a complex CMOS circuit. They will be required to identify and analyze the sources of switching power dissipation within the circuit, propose optimization techniques, and predict the potential power savings.

Criteria for Assessment (Total: 5 Marks):

- **Identification of Switching Power Sources (2 Marks)**:
  - Accurate identification of all key areas within the CMOS circuit where switching power dissipation occurs.
- **Proposed Optimization Techniques (2 Marks)**:
  - Thoughtful and feasible suggestions for minimizing switching power dissipation, including explanations of how these techniques would work in the given circuit.
- **Predicted Power Savings and Justification (1 Mark)**:
  - A reasoned estimation of the potential power savings from the proposed optimizations, supported by logical arguments or simple calculations.

End Semester Examination Marks (ESE):

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• 2 questions will be given from each module, out of which 1 question should be answered. Each question can have a maximum of 3 sub divisions. Each question carries 9 marks. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Analyse and evaluate power dissipation mechanisms in MOSFET devices, understand the need for low-power design, identify deep submicron transistor design challenges, and apply emerging technologies to optimize power efficiency in VLSI circuits.	**K3**
CO2	Identify and quantify various sources of power dissipation in digital ICs, including dynamic, short circuit, switching, glitching, and static power, and evaluate strategies for optimizing power consumption.	**K2**
CO3	Apply various low-power design approaches, including supply voltage scaling, architectural optimizations, and leakage power reduction techniques, to enhance power efficiency in VLSI circuits.	**K3**
CO4	Design and evaluate low-power circuits using various design styles, including non-clocked and clocked approaches, adiabatic switching, and energy recovery techniques, to effectively reduce power consumption in VLSI systems.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**3**	**3**		**1**				**1**	**1**		
CO2	**3**	**2**	**2**	**2**	**1**				**1**	**1**		
CO3	**3**	**3**	**3**		**2**				**1**	**1**		
CO4	**3**	**2**	**3**	**2**	**2**				**1**	**1**		

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Design of Analog CMOS Integrated Circuits	Behzad Razavi	McGraw-Hill	2/e, 2002
2	CMOS: Circuits Design, Layout and Simulation,	Baker, Li, Boyce,	Prentice Hall India,	1994
3	Microelectronic Circuits	Sedra & Smith	Oxford University Press	6/e,2017

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	CMOS Analog Circuit Design,	Phillip E. Allen, Douglas R. Holbery	Oxford University Press	3/e
2	Fundamentals of Microelectronics	Behzad Razavi	Wiley student Edition	2014
3	Analysis and Design of Analog Integrated Circuits	Meyer Gray , Hurst, Lewis	Wiley	5/e, 2009

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	www.youtube.com/@b_razavi, www.youtube.com/@analogicdesign-iitm5234
2	www.youtube.com/@b_razavi, www.youtube.com/@analogicdesign-iitm5234
3	www.youtube.com/@b_razavi, www.youtube.com/@analogicdesign-iitm5234
4	Switching Circuits and Logic Design by Prof. Indranil Sengupta Lectures 47-51

SEMESTER 7

RF MICROELECTRONICS

Course Code	PEEVT 751	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3-0-0-0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	None	Course Type	Theory

Course Objectives:

This Course aims

1. To provide an overview of passive components and lumped elements circuits.
2. To understand the fabrication of microwave integrated circuits.
3. To study various planar transmission lines.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Introduction to Passive Components, Inductors- printed inductors, wire inductors, resistors, capacitors, Monolithic capacitors, Via –holes and grounding. (No detailed analysis required). Lumped element circuits: Passive Circuits-filters and Couplers, Power dividers/ Combiners, Lumped Elements for biasing circuit, Phase Shifters, Digital Attenuators. (No detailed analysis required)	9
2	Microwave integrated circuit fabrication technology Introduction - Materials, Mask layout, Mask fabrication, Printed Circuit Boards- PCB Fabrication, PCB Inductors. Microwave Printed Circuits - MPC fabrication.	9

3	Hybrid integrated circuits Thin Film Technology, Thick film Technology- Coirfed Ceramic and Glass ceramic Technology. MMIC Fabrication, Steps Involved in the Fabrication of MOSFET, CMOS Fabrication, Micromachining fabrication.	**9**
4	Microstrip overview Introduction to Planar Transmission Line, Various types of planar transmission lines. Microstrip Lines, Introduction to Slot line and Coupled lines.	**9**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Discuss about the RF components and circuits.	**K2**
CO2	Explain about PCB fabrication.	**K2**
CO3	Understand MMIC Technology	**K2**
CO4	Explain about Microstrip Lines	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping od Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**	**2**										**2**
CO2	**3**	**2**										**2**
CO3	**3**	**2**										**2**
CO4	**3**	**2**										**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Radio Frequency Integrated Circuits and Technologies	Frank Ellinger	Springer	2007
2	Lumped Elements for RF and Microwave Circuits	Inder Bahl	Artech House	2003

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	RF Microelectronics	B.Razavi	Prentice-Hall PTR	1998
2	Microwave Integrated Circuits	Gupta K. C. &Amarjit Singh	John Wiley & Sons	1975
3	RFIC and MMIC Design and Technology	I.D Robertson,C .Lucyszyn	The Institution of Engineering and Technology	2001
4	Passive RF & Microwave Integrated Circuits	Leo G. Maloratsky	Elsevier	2004

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://youtu.be/cHbcdk-C4Zo?si=MAMALiV4ffGdQOAO
2	https://youtu.be/pgcqahZEdpY
3	https://youtu.be/lW0QMvmeVGs?si=lTNG13H6s1Jy-_Ip
4	https://youtu.be/ap9739K_OJo